Buoy Memory Management

# Introduction

This document details the flow of data between 4 SPI Flash Chips and the stm32l476RG Microcontroller. Flash storage is a fundamental component for high volume data. These chips will provide permanent storage to IMU Data (+- 2 – 10KB per set), GPS data (+- 25 bytes), Environmental Data (+- 8 bytes) and Power information. However, In order to optimize for performance and robustness, some form of data organization must be implemented for intelligent retrieval/ storage of data in a meaningful way. In addition, the system requires some form of back up should the device be unable to connect to the flash chips. The following document outlines the planning and implementation for such a system

# Flash Chips Physical Description

The flash Chips being used are AT45DB641E SPI Serial Flash Chips. Each chip can hold up to 64Mbit of data. Data can be read/ written at speeds of up to 85MHz of 15MHz in low power mode. The device is low power with high data retention requiring a supply voltage of 1.7V – 3.6V and draws a maximum of 11mA in Active Read mode thereby making it one of the lowest power consumption components in the system. In addition, the device comes with 2 x 256byte buffers that can store data while a read/ write operation is taking place. Memory is Organized into sectors (2 – 256 Kbs long), blocks (2kB long) and pages (256 bytes) with write, read and erase options at each level. The following diagrams are taken from the data sheet and show the architecture and memory organization of the chips

A screenshot of a social media post

Description automatically generated

Figure : Block diagram showing the architecture of the chip

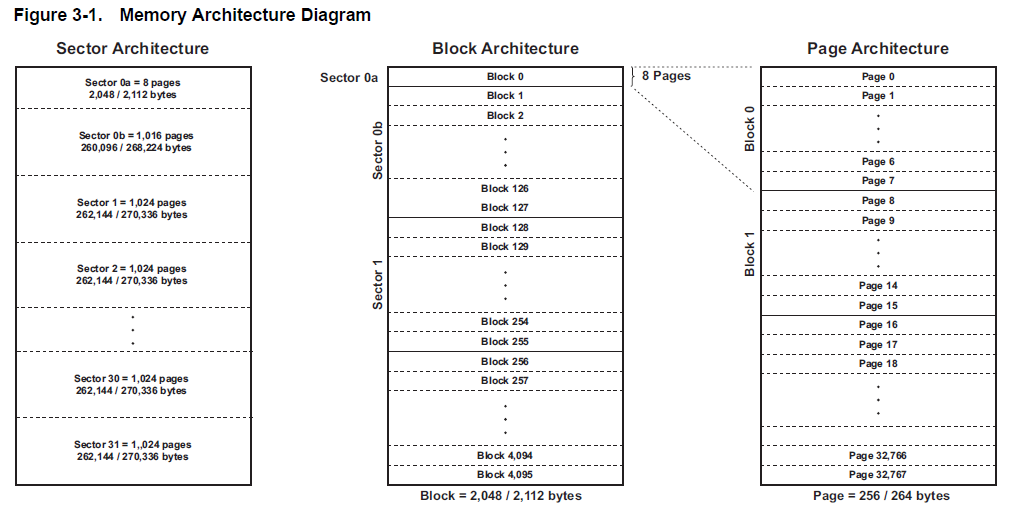


Figure : Memory Layout of Flash Chip Showing pages, sectors and blocks as well as sizes in bytes